THAT WHICH IS CLAIMED IS:

1. A phase changeable memory device comprising:

an integrated circuit substrate;

a first storage active region on the integrated circuit substrate having a first width;

a second storage active region on the integrated circuit substrate having a second width; and

a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds widths being less than a width of the transistor active region.

2. A device according to Claim 1 wherein the first width is equal to the second width and the first and second widths are about half of the width of the transistor active region.

3. A device according to Claim 1 further comprising a plurality of gate lines defining a plurality of rows of the phase changeable memory device, wherein a plurality of the first and second storage active regions are disposed alternately along the rows in a region between first and second gate lines of the plurality of gate lines and wherein the widths of the first and second storage active regions and the width of the transistor active region are parallel to the plurality of gate lines.

4. A device according to Claim 1 wherein the transistor active region comprises first and second sidewalls extending from a first end of the transistor active region to a second end of the transistor active region, wherein the first storage active region protrudes from the first sidewall of the transistor active region at the first end of the transistor active region and wherein the second storage region protrudes from the second sidewall of the transistor active region at the second end of the transistor active region.

5. A device according to Claim 1 wherein the transistor active region is a first transistor active region, the device further comprising:

a second transistor active region; and

a connector active region between the first transistor active region and the second transistor active region that electrically couples the first and second transistor active regions.

6. A device according to Claim 1 further comprising:

a first data storage element on the first storage active region;

a second data storage element on the second storage active region;

a first lower plug that electrically couples the first data storage element to the first storage active region; and

a second lower plug that electrically couples the second data storage element to the second data storage region.

7. A device according to Claim 6 further comprising:

a plurality of bit lines on the integrated circuit substrate;

a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

8. A device according to Claim 7:

wherein the first data storage element comprises a first barrier pattern that is electrically coupled to the first lower plug and a first phase changeable material pattern on the first barrier pattern;

wherein the second data storage element comprises a second barrier pattern that is electrically coupled to the second lower plug and a second phase changeable material pattern on the second barrier pattern; and

wherein the first and second upper plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

9. A device according to Claim 8 wherein a diameter of the first lower plug is larger than a diameter of the first upper plug and wherein a diameter of the second lower plug is larger than a diameter of the second upper plug.

10. A device according to Claim 8 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to the transistor active region.

11. A device according to Claim 10 further comprising an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source interconnection is disposed in the interlayer dielectric on the common source plug.

12. A device according to Claim 7:

wherein the first data storage element comprises a first phase changeable material pattern that is electrically coupled to the first lower plug and a first barrier pattern on the first phase changeable material pattern;

wherein the second data storage element comprises a second phase changeable material pattern that is electrically coupled to the second lower plug and a second barrier pattern on the second phase changeable material pattern; and

wherein the first and second lower plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

13. A device according to Claim 12 wherein a diameter of the first lower plug is less than a diameter of the first upper plug and wherein a diameter of the second lower plug is less than a diameter of the second upper plug.

14. A device according to Claim 12 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to the transistor active region.

15. A device according to Claim 14 further comprising an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source interconnection is disposed in the interlayer dielectric on the common source plug.

16. A device according to Claim 1 further comprising:

a first data storage element on the first storage active region;

a second data storage element on the second storage active region;

first and second lower plugs on the integrated circuit substrate;

a first buffer pattern on the first lower plug;

a second buffer pattern on the second lower plug;

a first intermediate plug on the first buffer pattern that electrically couples the first data storage element to the first storage active region; and

a second intermediate plug on the second buffer pattern that electrically couples the second data storage element to the second data storage region.

17. A device according to Claim 16 further comprising:

a plurality of bit lines on the integrated circuit substrate;

a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

18. A device according to Claim 17:

wherein the first data storage element comprises a first barrier pattern that is electrically coupled to the first intermediate plug and a first phase changeable material pattern on the first barrier pattern;

wherein the second data storage element comprises a second barrier pattern that is electrically coupled to the second intermediate plug and a second phase changeable material pattern on the second barrier pattern; and

wherein the first and second upper plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

19. A device according to Claim 18 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to the transistor active region.

20. A device according to Claim 19 further comprising an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source interconnection is disposed in the interlayer dielectric on the common source plug.

21. A device according to Claim 17:

wherein the first data storage element comprises a first phase changeable material pattern that is electrically coupled to the first intermediate plug and a first barrier pattern on the first phase changeable material pattern;

wherein the second data storage element comprises a second phase changeable material pattern that is electrically coupled to the second intermediate plug and a second barrier pattern on the second phase changeable material pattern; and

wherein the first and second intermediate plugs comprise heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

22. A device according to Claim 21 further comprising:

a common source interconnection on the integrated circuit substrate; and

a common source plug that electrically couples the common source interconnection to the transistor active region.

23. A device according to Claim 23 further comprising an interlayer dielectric on the integrated circuit substrate wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is dispose on the interlayer dielectric.

24. A method of fabricating a phase changeable memory device comprising:

forming a first storage active region on an integrated circuit substrate having a first width;

forming a second storage active region on the integrated circuit substrate having a second width; and

forming a transistor active region on the integrated circuit substrate between the first and second active regions, the first and seconds widths being less than a width of the transistor active region.

25. A method according to Claim 24 wherein the first width is equal to the second width and the first and second widths are about half of the width of the transistor active region.

26. A method according to Claim 24 further comprising forming a plurality of gate lines that define a plurality of rows of the phase changeable memory device, wherein a plurality of the first and second storage active regions being disposed alternately along the rows in a region between first and second gate lines of the plurality of gate lines and wherein the widths of the first and second storage active regions and the width of the transistor active region are parallel to the plurality of gate lines.

27. A method according to Claim 24 wherein forming the transistor active region comprises forming first and second sidewalls extending from a first end of the transistor active region to a second end of the transistor active region, wherein the first storage active region protrudes from the first sidewall of the transistor active region at the first end of the transistor active region and wherein the second storage region protrudes from the second sidewall of the transistor active region at the second end of the transistor active region.

28. A method according to Claim 24 wherein forming the transistor active region comprises forming a first transistor active region and a second transistor active region, the method further comprising forming a connector active region between the first transistor active region and the second transistor active region that electrically couples the first and second transistor active regions.

29. A method according to Claim 24 further comprising:

forming a first data storage element on the first storage active region;

forming a second data storage element on the second storage active region;

forming a first lower plug that electrically couples the first data storage element to the first storage active region; and

forming a second lower plug that electrically couples the second data storage element to the second data storage region.

30. A method according to Claim 29 further comprising:

forming a plurality of bit lines on the integrated circuit substrate;

forming a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

forming a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

31. A method according to Claim 30:

wherein forming the first data storage element comprises forming a first barrier pattern that is electrically coupled to the first lower plug and forming a first phase changeable material pattern on the first barrier pattern;

wherein forming the second data storage element comprises forming a second barrier pattern that is electrically coupled to the second lower plug and forming a second phase changeable material pattern on the second barrier pattern; and

wherein forming the first and second upper plugs comprises forming heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

32. A method according to Claim 31 wherein a diameter of the first lower plug is larger than a diameter of the first upper plug and wherein a diameter of the second lower plug is larger than a diameter of the second upper plug.

33. A method according to Claim 31 further comprising:

forming a common source interconnection on the integrated circuit substrate; and

forming a common source plug that electrically couples the common source interconnection to the transistor active region.

34. A method according to Claim 33 further comprising forming an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is disposed in the interlayer dielectric on the common source plug.

35. A method according to Claim 30:

wherein forming the first data storage element comprises forming a first phase changeable material pattern that is electrically coupled to the first lower plug and forming a first barrier pattern on the first phase changeable material pattern;

wherein forming the second data storage element comprises forming a second phase changeable material pattern that is electrically coupled to the second lower plug and forming a second barrier pattern on the second phase changeable material pattern; and

wherein forming the first and second lower plugs comprises forming heater plugs that

generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

36. A method according to Claim 35 wherein a diameter of the first lower plug is less than a diameter of the first upper plug and wherein a diameter of the second lower plug is less than a diameter of the second upper plug.

37. A method according to Claim 35 further comprising:

forming a common source interconnection on the integrated circuit substrate; and

forming a common source plug that electrically couples the common source interconnection to the transistor active region.

38. A method according to Claim 37 further comprising forming an interlayer dielectric on the integrated circuit substrate, wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is disposed in the interlayer dielectric on the common source plug.

39. A method according to Claim 24 further comprising:

forming a first data storage element on the first storage active region;

forming a second data storage element on the second storage active region;

forming first and second lower plugs on the integrated circuit substrate;

forming a first buffer pattern on the first lower plug;

forming a second buffer pattern on the second lower plug;

forming a first intermediate plug on the first buffer pattern that electrically couples the first data storage element to the first storage active region; and

forming a second intermediate plug on the second buffer pattern that electrically couples the second data storage element to the second data storage region.

40. A method according to Claim 39 further comprising:

forming a plurality of bit lines on the integrated circuit substrate;

forming a first upper plug that electrically couples a first bit line of the plurality of bit lines to the first data storage element; and

forming a second upper plug that electrically couples a second bit line of the plurality of bit lines to the second data storage element.

41. A method according to Claim 40:

wherein forming the first data storage element comprises forming a first barrier pattern that is electrically coupled to the first intermediate plug and forming a first phase changeable material pattern on the first barrier pattern;

wherein forming the second data storage element comprises forming a second barrier pattern that is electrically coupled to the second intermediate plug and forming a second phase changeable material pattern on the second barrier pattern; and

wherein forming the first and second upper plugs comprises forming heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

42. A method according to Claim 41 further comprising:

forming a common source interconnection on the integrated circuit substrate; and

forming a common source plug that electrically couples the common source interconnection to the transistor active region.

43. A method according to Claim 42 further comprising forming an interlayer dielectric on the integrated circuit substrate wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is dispose on the interlayer dielectric.

44. A method according to Claim 40:

wherein forming the first data storage element comprises forming a first phase changeable material pattern that is electrically coupled to the first intermediate plug and forming a first barrier pattern on the first phase changeable material pattern;

wherein forming the second data storage element comprises a second phase changeable material pattern that is electrically coupled to the second intermediate plug and forming a second barrier pattern on the second phase changeable material pattern; and

wherein forming the first and second intermediate plugs comprises forming heater plugs that generate heat to provide a phase transformation of the first phase changeable material pattern and the second phase changeable material pattern, respectively.

45. A method according to Claim 44 further comprising:

forming a common source interconnection on the integrated circuit substrate; and

forming a common source plug that electrically couples the common source interconnection to the transistor active region.

46. A method according to Claim 45 further comprising forming an interlayer dielectric on the integrated circuit substrate wherein the common source plug is disposed in the interlayer dielectric and wherein the common source plug is dispose on the interlayer dielectric.

47. A phase changeable memory device comprising:

an integrated circuit substrate;

a first storage active region on the integrated circuit substrate having a first cross sectional area;

a second storage active region on the integrated circuit substrate having a second cross sectional area; and

a transistor active region on the integrated circuit substrate between the first and second storage active regions, the first and seconds cross sectional areas being less than a cross sectional area of the transistor active region.